CLAIM AMENDMENTS

1. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, wherein the first housing portion includes a peripheral ledge, and the second housing portion is exposed ~~located~~ within the peripheral ledge ~~and is exposed~~; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

2. (Original) The device of claim 1, wherein the first housing portion contacts four outer side surfaces of the chip.

3. (Original) The device of claim 1, wherein the first housing portion is spaced from the upper surface.

4. (Original) The device of claim 1, wherein the second housing portion contacts the conductive trace.

5. (Original) The device of claim 1, wherein the second housing portion is spaced from the lower surface.

6. (Previously Presented) The device of claim 1, wherein the second housing portion is recessed relative to the peripheral ledge.

7. (Original) The device of claim 1, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

8. (Original) The device of claim 1, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

9. (Previously Presented) The device of claim 1, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

10. (Original) The device of claim 1, wherein the device is devoid of wire bonds, TAB leads and solder joints.

11. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell and is spaced from the lower surface; and

a conductive trace that extends laterally through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the first housing portion spans 360 degrees around the conductive trace at the opening.

12. (Previously Presented) The device of claim 11, wherein the second housing portion includes first and second opposing surfaces, the first surface contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

13. (Previously Presented) The device of claim 12, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

14. (Original) The device of claim 13, wherein the second housing portion is recessed relative to the peripheral ledge.

15. (Previously Presented) The device of claim 11, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

16. (Original) The device of claim 11, wherein the insulative housing consists of the first and second housing portions.

17. (Previously Presented) The device of claim 11, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

18. (Original) The device of claim 11, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

19. (Previously Presented) The device of claim 11, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

20. (Original) The device of claim 11, wherein the device is devoid of wire bonds, TAB leads and solder joints.

21. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and ~~uncurved~~ peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-

piece that contacts the chip, provides the peripheral side surfaces and the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, is farther from the bottom surface than the lower surface is from the bottom surface, does not extend across any of the peripheral side surfaces, provides at least a portion of the top surface, ~~and~~ is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

22. (Original) The device of claim 21, wherein the first housing portion contacts the lower surface and the outer side surfaces and is spaced from the upper surface.

23. (Original) The device of claim 21, wherein the second housing portion contacts the light sensitive cell and the conductive trace and is spaced from the lower surface.

24. (Original) The device of claim 21, wherein the first housing portion includes a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion is located within and recessed relative to the peripheral ledge.

25. (Previously Presented) The device of claim 21, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

26. (Original) The device of claim 21, wherein the insulative housing consists of the first and second housing portions.

27. (Previously Presented) The device of claim 21, wherein the light sensitive cell contacts a major surface of the second housing portion that faces towards and is parallel to the upper surface.

28. (Original) The device of claim 21, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

29. (Previously Presented) The device of claim 21, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

30. (Original) The device of claim 21, wherein the device is devoid of wire bonds, TAB leads and solder joints.

31. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive cell and is non-transparent, and the second housing portion is a single-piece or double-piece that provides a central portion of the top surface within the peripheral portion of the top surface, contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from the lower surface, is farther from the bottom surface than the lower surface is from the bottom surface, is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

32. (Previously Presented) The device of claim 31, wherein the second housing portion includes first and second opposing surfaces, the first surface faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and provides the central portion of the top surface and is exposed.

33. (Original) The device of claim 31, wherein the peripheral portion of the top surface forms a rectangular peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

34. (Original) The device of claim 33, wherein the peripheral ledge includes four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

35. (Original) The device of claim 31, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

36. (Original) The device of claim 31, wherein the insulative housing consists of the first and second housing portions.

37. (Previously Presented) The device of claim 31, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed.

38. (Original) The device of claim 31, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

39. (Previously Presented) The device of claim 31, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

40. (Original) The device of claim 31, wherein the device is devoid of wire bonds, TAB leads and solder joints.

41. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing further includes a

first insulative housing portion that covers the lower surface and is non-transparent and a second insulative housing portion that covers the light sensitive cell and is transparent; and

a conductive trace that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the conductive trace includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and the top surface.

42. (Original) The device of claim 41, wherein the first housing portion contacts the lower surface and four outer side surfaces of the chip.

43. (Original) The device of claim 41, wherein the second housing portion contacts the light sensitive cell and the conductive trace.

44. (Original) The device of claim 41, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

45. (Previously Presented) The device of claim 41, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

46. (Original) The device of claim 41, wherein the insulative housing consists of the first and second housing portions.

47. (Previously Presented) The device of claim 41, wherein the light sensitive cell contacts a major surface of the second housing portion that faces towards and is parallel to the upper surface.

48. (Original) The device of claim 41, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

49. (Previously Presented) The device of claim 41, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

50. (Original) The device of claim 41, wherein the device is devoid of wire bonds, TAB leads and solder joints.

51. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing further includes a first single-piece housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second single-piece housing portion that contacts the first housing portion and the conductive trace and is transparent, the first housing portion alone provides the bottom surface, and the first and second housing portions in combination provide the top surface; and

a conductive trace that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the conductive trace includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, wherein the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the top surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the top surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another.

52. (Previously Presented) The device of claim 51, wherein the second housing portion includes first and second opposing surfaces, the first surface contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

53. (Original) The device of claim 51, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

54. (Original) The device of claim 53, wherein the peripheral ledge includes four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

55. (Original) The device of claim 51, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

56. (Original) The device of claim 51, wherein the insulative housing consists of the first and second housing portions.

57. (Previously Presented) The device of claim 51, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

58. (Original) The device of claim 51, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

59. (Previously Presented) The device of claim 51, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

60. (Original) The device of claim 51, wherein the device is devoid of wire bonds, TAB leads and solder joints.

61. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends laterally through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the first housing portion spans 360 degrees around the conductive trace at the opening.

62. (Previously Presented) The device of claim 61, wherein the first housing portion contacts the lower surface and the side surfaces.

63. (Previously Presented) The device of claim 61, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

64. (Previously Presented) The device of claim 61, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

65. (Previously Presented) The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

66. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, is bent outside the insulative housing and is electrically connected to the pad inside the insulative housing.

67. (Previously Presented) The device of claim 66, wherein the first housing portion contacts the lower surface and the side surfaces.

68. (Previously Presented) The device of claim 66, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

69. (Previously Presented) The device of claim 66, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

70. (Previously Presented) The device of claim 66, wherein the device is devoid of wire bonds, TAB leads and solder joints.

71. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, does not contact an insulative material outside the first housing portion and is electrically connected to the pad inside the insulative housing.

72. (Previously Presented) The device of claim 71, wherein the first housing portion contacts the lower surface and the side surfaces.

73. (Previously Presented) The device of claim 71, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

74. (Previously Presented) The device of claim 71, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

75. (Previously Presented) The device of claim 71, wherein the device is devoid of wire bonds, TAB leads and solder joints.

76. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing, does not extend across any edge of the pad and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first housing portion, extends across one of the side surfaces and does not extend outside the insulative housing.

77. (Previously Presented) The device of claim 76, wherein the first housing portion contacts the lower surface and the side surfaces.

78. (Previously Presented) The device of claim 76, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

79. (Previously Presented) The device of claim 76, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one

another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

80. (Previously Presented) The device of claim 76, wherein the device is devoid of wire bonds, TAB leads and solder joints.

81. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first and second housing portions, extends across one of the side surfaces and does not extend outside the insulative housing.

82. (Previously Presented) The device of claim 81, wherein the first housing portion contacts the lower surface and the side surfaces.

83. (Previously Presented) The device of claim 81, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

84. (Previously Presented) The device of claim 81, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with

one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

85. (Previously Presented) The device of claim 81, wherein the device is devoid of wire bonds, TAB leads and solder joints.

86. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first and second housing portions, overlaps the pad, extends across one of the side surfaces and does not extend outside the insulative housing.

87. (Previously Presented) The device of claim 86, wherein the first housing portion contacts the lower surface and the side surfaces.

88. (Previously Presented) The device of claim 86, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

89. (Previously Presented) The device of claim 86, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

90. (Previously Presented) The device of claim 86, wherein the device is devoid of wire bonds, TAB leads and solder joints.

91. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

92. (Previously Presented) The device of claim 91, wherein the first housing portion contacts the lower surface and the outer side surfaces.

93. (Previously Presented) The device of claim 91, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

94. (Previously Presented) The device of claim 91, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

95. (Previously Presented) The device of claim 91, wherein the device is devoid of wire bonds, TAB leads and solder joints.

96. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

97. (Previously Presented) The device of claim 96, wherein the first housing portion contacts the lower surface and the outer side surfaces.

98. (Previously Presented) The device of claim 96, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

99. (Previously Presented) The device of claim 96, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

100. (Previously Presented) The device of claim 96, wherein the device is devoid of wire bonds, TAB leads and solder joints.

101. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive

cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

102. (Previously Presented) The device of claim 101, wherein the first housing portion contacts the lower surface and the outer side surfaces.

103. (Previously Presented) The device of claim 101, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

104. (Previously Presented) The device of claim 101, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

105. (Previously Presented) The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

106. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

107. (Previously Presented) The device of claim 106, wherein the first housing portion contacts the lower surface and the outer side surfaces.

108. (Previously Presented) The device of claim 106, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

109. (Previously Presented) The device of claim 106, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

110. (Previously Presented) The device of claim 106, wherein the device is devoid of wire bonds, TAB leads and solder joints.

111. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, is located between the second housing portion and the chip inside the insulative housing, is spaced from the top surface and is electrically connected to the pad inside the insulative housing.

112. (Previously Presented) The device of claim 111, wherein the first housing portion contacts the lower surface and the outer side surfaces.

113. (Previously Presented) The device of claim 111, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

114. (Previously Presented) The device of claim 111, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are

adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

115. (Previously Presented) The device of claim 111, wherein the device is devoid of wire bonds, TAB leads and solder joints.

116. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing, includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

117. (Previously Presented) The device of claim 116, wherein the first housing portion contacts the lower surface and the outer side surfaces.

118. (Previously Presented) The device of claim 116, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

119. (Previously Presented) The device of claim 116, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

120. (Previously Presented) The device of claim 116, wherein the device is devoid of wire bonds, TAB leads and solder joints.

121. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

122. (Previously Presented) The device of claim 121, wherein the first housing portion contacts the lower surface and the outer side surfaces.

123. (Previously Presented) The device of claim 121, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

124. (Previously Presented) The device of claim 121, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

125. (Previously Presented) The device of claim 121, wherein the device is devoid of wire bonds, TAB leads and solder joints.

126. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top

surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

127. (Previously Presented) The device of claim 126, wherein the first housing portion contacts the lower surface and the outer side surfaces.

128. (Previously Presented) The device of claim 126, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

129. (Previously Presented) The device of claim 126, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

130. (Previously Presented) The device of claim 126, wherein the device is devoid of wire bonds, TAB leads and solder joints.

131. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces

and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

132. (Previously Presented) The device of claim 131, wherein the first housing portion contacts the lower surface and the outer side surfaces.

133. (Previously Presented) The device of claim 131, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

134. (Previously Presented) The device of claim 131, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

135. (Previously Presented) The device of claim 131, wherein the device is devoid of wire bonds, TAB leads and solder joints.

136. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

137. (Previously Presented) The device of claim 136, wherein the first housing portion contacts the lower surface and the outer side surfaces.

138. (Previously Presented) The device of claim 136, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

139. (Previously Presented) The device of claim 136, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

140. (Previously Presented) The device of claim 136, wherein the device is devoid of wire bonds, TAB leads and solder joints.

141. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, ~~uncurved~~ peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip, does not extend across any of the peripheral side surfaces, ~~and~~ is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

142. (Previously Presented) The device of claim 141, wherein the first housing portion contacts the lower surface and the outer side surfaces.

143. (Previously Presented) The device of claim 141, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

144. (Previously Presented) The device of claim 141, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one

another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

145. (Previously Presented) The device of claim 141, wherein the device is devoid of wire bonds, TAB leads and solder joints.

146. (Previously Presented) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

147. (Previously Presented) The device of claim 146, wherein the first housing portion contacts the lower surface and the outer side surfaces.

148. (Previously Presented) The device of claim 146, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

149. (Previously Presented) The device of claim 146, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

150. (Previously Presented) The device of claim 146, wherein the device is devoid of wire bonds, TAB leads and solder joints.

151. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is recessed relative to the peripheral ledge; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

152. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

153. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing, and the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that

face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

154. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.